



Spoke 1- Future HPC Publication list

WP1 - Flagship 1, Resp. POLITO

[1]

2024 Davide Baroffio, Federico Reghenzani, and William Fornaciari. **Enhanced Compiler Technology for Software-based Hardware Fault Detection**. In: ACM Trans. Des. Autom. Electron. Syst. 29.5. ISSN: 1084-4309 [doi: 10.1145/3660524](https://doi.org/10.1145/3660524).

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2024 Enrico Bini and Valérie Berthé. **SimPFair: tight fairness at low cost**. In: The 32nd International Conference on Real- Time Networks and Systems (RTNS 2024). Porto, Portugal. doi: [10.1145/3696355.3699705](https://doi.org/10.1145/3696355.3699705).

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2024 Michele Castrovilli and Enrico Bini. **SlackCheck: A Linux Kernel Module to Verify Temporal Properties of a Task Schedule**. In: 36th Euromicro Conference on Real-Time Systems (ECRTS 2024), 2:1–2:24. [doi: 10.4230/LIPIcs.ECRTS.2024.2](https://doi.org/10.4230/LIPIcs.ECRTS.2024.2).

[4]

2024 Junchao Chen, Giuseppe Esposito, Fernando Fernandes dos Santos, Juan-David Guerrero-Balaguera, Angeliki Kritikakou, Milos Krstic, Robert Limas, Josie E Rodriguez Condia, Matteo Sonza Reorda, Marcello Traiola, et al. **Reliability Assessment of Large DNN Models: Trading Off Performance and Accuracy**. In: IFIP/IEEE International Conference on Very Large Scale Integration. DOI: [10.1109/VLSI-SoC62099.2024.10767814](https://doi.org/10.1109/VLSI-SoC62099.2024.10767814)

[5]

2024 Josie E. Rodriguez Condia, Juan-David Guerrero-Balaguera, Robert Limas Sierra, and Matteo Sonza Reorda. **Analyzing the Structural and Operational Impact of Faults in Floating-Point and Posit Arithmetic Cores for CNN Operations**. In: 2024 IEEE European Test Symposium (ETS), pp. 1–4. [doi: 10.1109/ETS61313.2024.10567884](https://doi.org/10.1109/ETS61313.2024.10567884).

[6]

2024 S. Cretì, M. Omaña, C. Metra, and G. Borelli. **Reliability of AI in Predicting the State of Health of Li-Ion Batteries**. In: Proc. of the 30th IEEE Int. Symp. on On-Line Testing and Robust System Design, Rennes (France) (IOLTS 2024). DOI: [10.1109/IOLTS60994.2024.10616089](https://doi.org/10.1109/IOLTS60994.2024.10616089)



[7]

2024 Giuseppe Esposito, Juan-David Guerrero-Balaguera, Josie E. Rodriguez Condia, Marco Levorato, and Matteo Sonza Reorda. **Enhancing the Reliability of Split Computing Deep Neural Net-works**. In: 2024 IEEE 30th International Symposium on On-Line Testing and Robust System Design (IOLTS), pp. 1–7.

[doi: 10.1109/IOLTS60994.2024.10616071](https://doi.org/10.1109/IOLTS60994.2024.10616071)

[8]

2024 Giuseppe Esposito, Juan-David Guerrero-Balaguera, Josie E. Rodriguez Condia, Marco Levorato, and Matteo Sonza Reorda. **Assessing the Reliability of Different Split Computing Neural Network Applications**. In: 25th IEEE Latin-American Test Symposium (LATS 2024), pp. 1–6. DOI: [10.1109/LATS62223.2024.10534618](https://doi.org/10.1109/LATS62223.2024.10534618)

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2024 Dennis Gnad, Martin Gotthard, Jonas Krautter, Angeliki Kritikakou, Vincent Meyers, Paolo Rech, Josie E. Rodriguez Condia, Annachiara Ruospo, Ernesto Sanchez, Fernando Fernandes Dos Santos, Olivier Sentieys, Mehdi Tahoori, Russell Tessier, and Marcello Traiola. **Reliability and Security of AI Hardware**. In: 2024 IEEE European Test Symposium (ETS), pp. 1–10.

[doi: 10.1109/ETS61313.2024.10567471](https://doi.org/10.1109/ETS61313.2024.10567471)

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2024 J. Guerrero-Balaguera, J. E. R. Condia, Levorato M., and M. Sonza Reorda. **Evaluating the Reliability of Supervised Compression for Split Computing**. In: 42nd IEEE VLSI Test Symposium (VTS 2024), pp. 1–6. DOI: [10.1109/VTS60656.2024.10538938](https://doi.org/10.1109/VTS60656.2024.10538938)

[11]

2024 G. Laccetti, M. Lapegna, R. Montella, and D. Romano. **Striking Trade-off Between High Performance and Energy Efficiency in an Edge Computing Application for Detecting Floating Plastic Debris**. In: Proc. Workshop on Flexible Resource and Application Management on the Edge (FRAME2024). ACM, New York (USA), pp. 51–58.

[doi: 10.1145/3659994.3660309](https://doi.org/10.1145/3659994.3660309)

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2024 R. Limas Sierra, J. Guerrero-Balaguera, F. Pessia, J. E. R. Condia, and M. Sonza Reorda. **Analyzing the Impact of Scheduling Policies on the Reliability of GPUs Running CNN Operations**. In: 42nd IEEE VLSI Test Symposium (VTS 2024), pp. 1–6.

DOI: [10.1109/VTS60656.2024.10538940](https://doi.org/10.1109/VTS60656.2024.10538940)



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2024 R. Limas Sierra, Juan-David Guerrero-Balaguera, Josie E. Rodriguez Condia, and Matteo Sonza Reorda. **Exploring Hardware Fault Impacts on Different Real Number Representations of the Structural Resilience of TCUs in GPUs**. In: Electronics 13.3. ISSN: 2079-9292.
[doi: 10.3390/electronics13030578](https://doi.org/10.3390/electronics13030578)

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2024 Robert Alexander Limas Sierra, Juan-David Guerrero-Balaguera, Josie E Rodriguez Condia, and Matteo SONZA REORDA. **Analyzing the Reliability of TCUs Through Micro-architecture and Structural Evaluations for Two Real Number Formats**. In: VLSI-SoC 2023: Silicon Innovations for Trustworthy Artificial Intelligence. Springer.
DOI: [10.1109/VLSI-SoC57769.2023.10321881](https://doi.org/10.1109/VLSI-SoC57769.2023.10321881)

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2024 Gabriele Mencagli, Massimo Torquati, Dalvan Griebler, Alessandra Fais, and Marco Danelutto. **General-purpose data stream processing on heterogeneous architectures with WindFlow**. In: Journal of Parallel and Distributed Computing 184, p. 104782. ISSN: 0743-7315.
[doi: 10.1016/j.jpdc.2023.104782](https://doi.org/10.1016/j.jpdc.2023.104782).

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2024 M. Omaña, F. Cantagallo, F. Finelli, and C. Metra. **AI for Cyberattacks' Detection in the Metaverse**. In: Proceedings of IEEE International Symposium on the Emerging Metaverse (ISEMV2024), Bellevue (WA). <https://hdl.handle.net/11585/993398>

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2024 M. Omaña, A. Manfredi, C. Metra, R. Locatelli, M. Chiavacci, and S. Petrucci. **Data Centers' Reliability Risks due to Faults Affecting their High Performance Microprocessors**. In: 1st IEEE RAS in Data Centers Summit (RAS 2024), Santa Clara (CA), June 11-12.

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2024 M. Omaña, A. Manfredi, C. Metra, R. Locatelli, M. Chiavacci, and S. Petrucci. **Silent Data Corruption and Reliability Risks due to Faults Affecting High Performance Microprocessors' Caches**. In: Proc. of the 30th IEEE Int. Symp. on On-Line Testing and Robust System Design, Rennes (France) (IOLTS 2024).
DOI: [10.1109/IOLTS60994.2024.10616059](https://doi.org/10.1109/IOLTS60994.2024.10616059)



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2024 Francesco Paladino, Alessandro Biondi, Enrico Bini, and Paolo Pazzaglia. **Optimizing Per-Core Priorities to Minimize End-To-End Latencies**. In: 36th Euromicro Conference on Real-Time Systems (ECRTS 2024). Dagstuhl, Germany, 6:1–6:25.

[doi: 10.4230/LIPIcs.ECRTS.2024.6](https://doi.org/10.4230/LIPIcs.ECRTS.2024.6)

[20]

2024 Francesco Pessia, Juan-David Guerrero-Balaguera, Robert Limas Sierra, Josie E. Rodriguez Condia, Marco Levorato, and Matteo Sonza Reorda. **Effective Application-level Error Modeling of Permanent Faults on AI Accelerators**. In: 2024 IEEE 30th International Symposium on On-Line Testing and Robust System Design (IOLTS), pp. 1–7.

[doi: 10.1109/IOLTS60994.2024.10616087](https://doi.org/10.1109/IOLTS60994.2024.10616087)

[21]

2024 Maria Luisa Pinto-Salamanca, Josie E. Rodriguez Condia, J. A. Hidalgo-Lopez, and Wilson-Javier Perez H. **Analyzing the Reliability of Stream Sparse Matrix-Vector Multiplication Accelerators: A High-Level Approach**. In: 25th IEEE Latin-American Test Symposium (LATS 2024), pp. 1–4.

DOI: [10.1109/LATS62223.2024.10534624](https://doi.org/10.1109/LATS62223.2024.10534624)

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2024 F. Reghenzani and W. Fornaciari. **Towards Certifiable Software-Implemented Hardware Fault Tolerance**. In: Proceedings of IEEE 14th International Symposium on Industrial Embedded Systems (SIES), p. 7.

DOI: [10.1109/SIES57906.2024.00010](https://doi.org/10.1109/SIES57906.2024.00010)

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2024 Josie E Rodriguez Condia, Juan-David Guerrero-Balaguera, Edwar J Patiño Núñez, Robert Limas, and Matteo Sonza Reorda. **Investigating and Reducing the Architectural Impact of Transient Faults in Special Function Units for GPUs**. In: Journal of Electronic Testing, pp. 1–14.

DOI: [10.1007/s10836-024-06107-9](https://doi.org/10.1007/s10836-024-06107-9)

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2024 Mahdi Taheri, Mohammad Hasan Ahmadilivani, Maksim Jenihhin, Jaan Raik, Salvatore Papalardo, Alberto Bosio, Bastien Deveautour, Fernando F. dos Santos, Marcello Traiola, Angeliki kritikakou, Robert Limas Sierra, Juan-David Guerrero-Balaguera, Josie E. Rodriguez Condia, and Matteo Sonza Reorda. **Special Session: Reliability Assessment Recipes for DNN Accelerators**. In: 42nd IEEE VLSI Test Symposium (VTS 2024), pp. 1–10.

DOI: [10.1109/VTS54335.2024.00010](https://doi.org/10.1109/VTS54335.2024.00010)



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2024 M. Zhupa, M. Naldi, M. Omaña, and C. Metra. **On the Reliability of Clock Monitoring Units of Microcontrollers for Safety Critical Applications**. In: Proc. of the 30th IEEE Int. Symp. on On-Line Testing and Robust System Design, Rennes (France) (IOLTS 2024).

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2023 Davide Baroffio and Federico Reghenzani. **Compiler-Injected SIHFT for Embedded Operating Systems**. In: Proceedings of the 20th ACM International Conference on Computing Frontiers. CF '23. Bologna, Italy: Association for Computing Machinery, pp. 337–343. ISBN: 9798400701405.

[doi: 10.1145/3587135.3589944](https://doi.org/10.1145/3587135.3589944).

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2023 Enrico Bini, Paolo Pazzaglia, and Martina Maggio. **Zero-Jitter Chains of Periodic LET Tasks via Algebraic Rings**. In: IEEE Transactions on Computers 72.11, pp. 3057–3071.

DOI: [10.1109/TC.2023.3234567](https://doi.org/10.1109/TC.2023.3234567)

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2023 Lia Cagnizi, Federico Reghenzani, and William Fornaciari. **Poster Abstract: Run-time Dynamic WCET Estimation**. In: Proceedings of the 8th ACM/IEEE Conference on Internet of Things Design and Implementation. IoTDI '23. , San Antonio, TX, USA, Association for Computing Machinery, pp. 458–460. ISBN: 9798400700378.

[doi: 10.1145/3576842.3589168](https://doi.org/10.1145/3576842.3589168)

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2023 J. E. R. Condia, Nikolaos I. Deligiannis, Jacopo Sini, Riccardo Cantoro, and Matteo Sonza Reorda. **Functional Testing with STLs: A Step Towards Reliable RISC-V-based HPC Commodity Clusters**. In: High Performance Computing. Ed. by Amanda Bienz, Michèle Weiland, Marc Baboulin, and Carola Kruse. Springer Nature Switzerland, pp. 444–457. ISBN: 978-3-031-40843-4.

DOI: [10.1007/978-3-031-40844-1_34](https://doi.org/10.1007/978-3-031-40844-1_34)

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2023 J. E. R. Condia, J. Guerrero-Balaguera, E. J. Patino Nunez, R. Limas Sierra, and M. Sonza Reorda. **Analyzing the Architectural Impact of Transient Fault Effects in SFUs of GPUs**. In: 24th IEEE Latin-American Test Symposium (LATS2023), pp. 1–6. DOI:

[10.1109/LATS57523.2023.10124567](https://doi.org/10.1109/LATS57523.2023.10124567)

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2023 J. E. R. Condia, J. Guerrero-Balaguera, E. J. Patino Nunez, R. Limas Sierra, and M. Sonza Reorda. **Evaluating the Prevalence of SFUs in the Reliability of GPUs**. In: 28th IEEE European Test Symposium (ETS2023), pp. 1–6. DOI: [10.1109/ETS2023.10124568](https://doi.org/10.1109/ETS2023.10124568)

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2023 Cacciapuoti R. D'Amore L., **Scalability analysis of a two-level domain decomposition approach in space and time solving data assimilation models**. In: Concurrency and Computation: Practice and Experience 36, art. N. 7937. DOI: [10.1002/cpe.7937](https://doi.org/10.1002/cpe.7937)

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2023 Cacciapuoti R. D'Amore L., **Sensitivity Analysis of the Data Assimilation-Driven Decomposition in Space and Time to Solve PDE-Constrained Optimization Problems**. In: Axiom - MDPI 12.6, art. N. 541. DOI: [10.3390/axioms12060541](https://doi.org/10.3390/axioms12060541)

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2023 Cacciapuoti R. D'Amore L., **Space-Time Decomposition of Kalman Filter**. In: Numerical Mathematics 16.4, pp. 847–882. DOI: [10.1007/s11075-023-01234-5](https://doi.org/10.1007/s11075-023-01234-5)

[35]

2023 M. Danelutto, G. Mencagli, A. Ottimo, F. Iannone, and P. Palazzari. **FastFlow targeting FPGAs**. In: 2023 31st Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP), pp. 104–108.
[doi: 10.1109/PDP59025.2023.00023](https://doi.org/10.1109/PDP59025.2023.00023).

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2023 G. De Lucia, M. Lapegna, and D. Romano. **A GPU Accelerated Hyperspectral 3D Convolutional Neural Network Classification at the Edge with Principal Component Analysis Preprocessing**. In: Parallel Processing and Applied Mathematics. 14th International Conference, PPAM 2022, Gdansk, Poland, September 11–14, 2022 Revised Selected Papers, Part II. Vol. 13827. Lecture Notes in Computer Science. Springer, Cham, Switzerland, pp. 127–138. DOI: [10.1007/978-3-031-24802-3_12](https://doi.org/10.1007/978-3-031-24802-3_12)

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2023 G. De Lucia, M. Lapegna, and D. Romano. **Unlocking the Potential of Edge Computing for Hyperspectral Image Classification: An Efficient Low-Energy Strategy**. In: Future Generation Computing Systems 147, pp. 207–218. DOI: [10.1016/j.future.2023.05.012](https://doi.org/10.1016/j.future.2023.05.012)

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2023 T. Faller, N. I. Deligiannis, M. Schwörer, M. Sonza Reorda, and B. Becker. **Constraint-Based Automatic SBST Generation for RISC-V Processor Families**. In: 28th IEEE European Test Symposium (ETS2023), pp. 1–6. DOI: [10.1109/ETS2023.10124569](https://doi.org/10.1109/ETS2023.10124569)

[39]

2023 William Fornaciari, Federico Reghenzani, Federico Terraneo, Davide Baroffio, Cecilia Metra, Martin Omana, Josie E. Rodriguez Condia, Matteo Sonza Reorda, Robert Birke, Iacopo Colonnelli, Gianluca Mittone, Marco Aldinucci, Gabriele Mencagli, Francesco Iannone, Filippo Palombi, Giuseppe Zummo, Daniele Cesarini, and Federico Tesser. **RISC-V-Based Platforms for HPC: Analyzing Non-functional Properties for Future HPC and Big-Data Clusters**. In: Embedded Computer Systems: Architectures, Modeling, and Simulation. Ed. by Cristina Silvano, Christian Pilato, and Marc Reichenbach. Cham: Springer Nature Switzerland, pp. 395–410. ISBN: 978-3-031-46077-7. DOI: https://dx.doi.org/10.1007/978-3-031-46077-7_26

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2023 Andrea Galimberti, Gabriele Montanaro, William Fornaciari, and Davide Zoni. **An Evaluation of the State-Of-The-Art Software and Hardware Implementations of BIKE**. In: 14th Workshop on Parallel Programming and Run-Time Management Techniques for Many-Core Architectures and 12th Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms, PARMA-DITAM 2023, January 17, 2023, Toulouse, France. Ed. by João Bispo, Henri-Pierre Charles, Stefano Cherubin, and Giuseppe Massari. Vol. 107. OASICS. Schloss Dagstuhl - Leibniz-Zentrum für Informatik, 4:1–4:12.

[doi: 10.4230/OASICS.PARMA-DITAM.2023.4](https://doi.org/10.4230/OASICS.PARMA-DITAM.2023.4)

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2023 Guerrero-Balaguera J., Condia J. E. R., Fernandes dos Santos F., Sonza Reorda M., and Rech P. **Understanding the Effects of Permanent Faults in GPU's Parallelism Management and Control Units**. In: The International Conference for High Performance Computing, Networking, Storage, and Analysis (SC'23), pp. 1–12.

[doi: 10.1145/3581784.3607086](https://doi.org/10.1145/3581784.3607086)

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2023 M. Lapeгна, V. Mele, and D. Romano. **Clustering Algorithms for Enhanced Trustworthiness on High Performance Edge Computing Devices**. In: Electronics - MDPI 12.7, art. N. 1689.

[doi: 10.3390/electronics12071689](https://doi.org/10.3390/electronics12071689)

[43]

2023 R. Limas Sierra, J. Guerrero-Balaguera, J. E. R. Condia, and M. Sonza Reorda. **A Reliability-aware Environment for Design Exploration for GPU Devices**. In: 26th International Symposium



on Design and Diagnostics of Electronic Circuits and Systems (DDECS2023), pp. 1–6.

DOI: [10.1109/DDECS57882.2023.10139643](https://doi.org/10.1109/DDECS57882.2023.10139643)

[44]

2023 R. Limas Sierra, J. Guerrero-Balaguera, J. E. R. Condia, and M. Sonza Reorda. **Analyzing the Impact of Different Real Number Formats on the Structural Reliability of TCUs in GPUs.** In: 31st IFIP/IEEE Conference on Very Large Scale Integration (VLSI-SoC), pp. 1–6.

DOI: [10.1109/VLSI-SoC57769.2023.10321881](https://doi.org/10.1109/VLSI-SoC57769.2023.10321881)

[45]

2023 R. Limas Sierra, J. Guerrero-Balaguera, J. E. R. Condia, and M. Sonza Reorda. **Optimizing the Analysis and Evaluation of Logic Simulation Workloads in HPC Systems.** In: 17th IEEE International Conference on Application of Information and Communication Technologies (AICT), pp. 1–6. DOI: [10.1109/AICT59525.2023.10313156](https://doi.org/10.1109/AICT59525.2023.10313156)

[46]

2023 Giuseppe Massari, Miriam Peta, Alessandro Campi, Federico Reghenzani, Federico Terraneo, Giovanni Agosta, William Fornaciari, Sebastian Ciesielski, Michal Kulczewski, and Wojciech Piatek. **Reliability-oriented resource management for High-Performance Computing.** In: Sustainable Computing: Informatics and Systems 39, p. 100873. ISSN: 2210-5379.

doi: [10.1016/j.suscom.2023.100873](https://doi.org/10.1016/j.suscom.2023.100873)

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2023 V. Mele and G. Laccetti., **Algorithm and Software Overhead: A Theoretical Approach to Performance Portability.** In: Parallel Processing and Applied Mathematics. 14th International Conference, PPAM 2022 Gdansk, Poland, September 11–14, 2022 Revised Selected Papers, Part II. Vol. 13827. Lecture Notes in Computer Science. Springer, Cham, Switzerland, pp. 89–100. DOI:

https://doi.org/10.1007/978-3-031-30445-3_8

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2023 Alberto Ottimo, Gabriele Mencagli, and Marco Danelutto. **FSP: a Framework for Data Stream Processing Applications targeting FPGAs.** In: 2023 31st Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP), pp. 92–99.

doi: [10.1109/PDP59025.2023.00021](https://doi.org/10.1109/PDP59025.2023.00021)

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2023 Federico Reghenzani, Zhishan Guo, and William Fornaciari. **Software Fault Tolerance in Real-Time Systems: Identifying the Future Research Questions.** In: ACM Comput. Surv. 55.14s. ISSN: 0360-0300.

doi: [10.1145/3589950](https://doi.org/10.1145/3589950).



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2023 S. Saeedi, A. Savino, and S. Di Carlo. **Design Space Exploration of Approximate Computing Techniques with a Reinforcement Learning Approach**. In: The 53rd Annual IEEE/IFIP International Conference on Dependable Systems and Networks Workshop (DSN-W'23). IEEE. DOI: [10.1109/DSN-W58399.2023.00047](https://doi.org/10.1109/DSN-W58399.2023.00047)

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2023 M. Sonza Reorda, R Cantoro, Josie E Rodriguez Condia, A Ruospo, and E Sanchez. **Self-Test Libraries for RISC-V safety-critical applications: recent advances**. In: RISC-V Europe Summit 2023. <https://riscv-europe.org/summit/2023/posters>



WP2 (Flagship 2, Resp. POLIMI)

[52]

Cristina Silvano, Daniele Ielmini, Fabrizio Ferrandi, Leandro Fiorin, Serena Curzel, Luca Benini, Francesco Conti, Angelo Garofalo, Cristian Zambelli, Enrico Calore, Sebastiano Fabio Schifano, Maurizio Palesi, Giuseppe Ascia, Davide Patti, Stefania Perri, Nicola Petra, Davide De Caro, Luciano Lavagno, Teodoro Urso, Valeria Cardellini, Gian Carlo Cardarilli, Robert Birke, **A Survey on Deep Learning Hardware Accelerators for Heterogeneous HPC Platforms**. Jun 2023, Major Revision ACM CSUR.

[doi: 10.48550/arXiv.2306.15552](https://doi.org/10.48550/arXiv.2306.15552)

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Fabrizio Ferrandi, Serena Curzel, Leandro Fiorin, Daniele Ielmini, Cristina Silvano, Francesco Conti, Alessio Burrello, Francesco Barchi, Luca Benini, Luciano Lavagno, Teodoro Urso, Enrico Calore, Sebastiano Fabio Schifano, Cristian Zambelli, Maurizio Palesi, Giuseppe Ascia, Davide Patti, Stefania Perri, Nicola Petra, Davide De Caro, Gennaro di Meo, Valeria Cardellini, Salvatore Filippone, Francesco Lo Presti, Francesco Silvestri, Paolo Palazzari, **A Survey on Design Methodologies for Accelerating Deep Learning on Heterogeneous Architectures**. Nov. 2023, Submitted to ACM CSUR (In Review)

[doi: 10.48550/arXiv.2306.15552](https://doi.org/10.48550/arXiv.2306.15552)

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Zambelli, C., Miola, A., Calore, E., Micheloni, R., Schifano, S.F. (2024). **Computational Storage for 3D NAND Flash Error Recovery Flow Prediction**. In: Ciofi, C., Limiti, E. (eds) Proceedings of SIE 2023. SIE 2023. Lecture Notes in Electrical Engineering, vol 1113. Springer, Cham.

[doi: 10.1007/978-3-031-48711-8_51](https://doi.org/10.1007/978-3-031-48711-8_51)

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H. Aziza, C. Zambelli, S. Hamdioui, S. Diware, R. Bishnoi and A. Gebregiorgis, **On the Reliability of RRAM-Based Neural Networks**, 2023 IFIP/IEEE 31st International Conference on Very Large Scale Integration (VLSI-SoC), Dubai, United Arab Emirates, 2023, pp. 1-8.

[doi: 10.1109/VLSI-SoC57769.2023.10321859](https://doi.org/10.1109/VLSI-SoC57769.2023.10321859)

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Stefania Perri, **Deep Learning Hardware Accelerators for Heterogeneous HPC Platforms: An Early Survey of the Flagship2 Project of the Italian National Center on HPC**, Presented at FPL 2023.

https://docs.google.com/presentation/d/1uewZVYDX7qXFH6jj_qo00Xpil8edWlwV/edit#slide=id.p1



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F. Spagnolo, P. Corsonello, F. Frustaci and S. Perri, **Design of a Low-Power Super-Resolution Architecture for Virtual Reality Wearable Devices**, in *IEEE Sensors Journal* (Received the best paper award), vol. 23, no. 8, pp. 9009-9016, 15 April, 2023.

[doi: 10.1109/JSEN.2023.3256524](https://doi.org/10.1109/JSEN.2023.3256524)

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Sestito, C., Perri, S. & Stewart, R., **FPGA Design of Transposed Convolutions for Deep Learning Using High-Level Synthesis**. *J Sign Process Syst* 95, 1245–1263 (2023).

[doi: 10.1007/s11265-023-01883-7](https://doi.org/10.1007/s11265-023-01883-7)

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Spagnolo, F., Corsonello, P., Frustaci, F. et al., **Approximate bilateral filters for real-time and low-energy imaging applications on FPGAs**. *J Supercomput* 80, 15894–15916 (2024).

[doi: 10.1007/s11227-024-06084-y](https://doi.org/10.1007/s11227-024-06084-y)

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M. U. Jamal, Z. Li, M. T. Lazarescu and L. Lavagno, **A Graph Neural Network Model for Fast and Accurate Quality of Result Estimation for High-Level Synthesis**, in *IEEE Access*, vol. 11, pp. 85785-85798, 2023,

[doi: 10.1109/ACCESS.2023.3303840](https://doi.org/10.1109/ACCESS.2023.3303840).

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Shiyuan Deng, Francesco Silvestri, and Yufei Tao. **Enumerating Subgraphs of Constant Sizes in External Memory**. In 26th International Conference on Database Theory (ICDT 2023). Leibniz International Proceedings in Informatics (LIPIcs), Volume 255, pp. 4:1-4:20, Schloss Dagstuhl – Leibniz-Zentrum für Informatik (2023). Received best paper award.

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